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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,528	10/06/2000	Andrew K. Percy	X-444-2P-2 US	1500

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XILINX, INC  
ATTN: LEGAL DEPARTMENT  
2100 LOGIC DR  
SAN JOSE, CA 95124

EXAMINER

AHN, SAM K

ART UNIT PAPER NUMBER

2634

DATE MAILED: 06/07/2004

20

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/684,528

Applicant(s)

PERCEY ET AL.

Examiner

Sam K. Ahn

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on amendment, received on 3/3/04.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4, 6 and 7 is/are allowed.
- 6) ☒ Claim(s) 8, 9 and 17-21 is/are rejected.
- 7) ☒ Claim(s) 10-16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 8, 9 and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuzaki (cited previously).

Regarding claims 8 and 20, Matsuzaki discloses a method for spreading the electromagnetic emissions of a generated clock signal that is created in response to a reference clock signal (see Fig.14), comprising the steps of providing a delay line (11, 13) in the path of the reference clock signal, providing an adjustable delay trim units or plurality of selectable delay trim units (570~574 in Fig.17) in the path of the reference clock signal, enabling a first, second, third, fourth and fifth set of delay trim units in the delay adjustable delay line during its respective clock period where the control signals (Q0~Q4) enables corresponding delay elements and adjusts the clock period. The control signals (Q0~Q4) are predetermined patterns (see Fig.18) being sent to the variable delay circuits (11,13) to adjust the delay line. By the output of the phase comparator (16) the control signals (Q0~Q4) adjusts the delay elements. Matsuzaki further discloses that the phase relations are predetermined with relation to the control signals

shown in Fig.18. When the control signals are received by the controller (26 in Fig.14), a predetermined pattern (11111, 11110, 11101, 11100 ... and so on) are sent to the delay elements to adjust the delay elements or trim units.

These patterns can further be interpreted as a repeating regular pattern since the patterns are not irregular or not known by the delay elements when received, and are repeated by the up and down converter depending on the phase relation detected by the phase detector. The patterns, as shown in Fig.18, may be repeated continuously to adjust the repeating clock cycle during successive clock cycles or continuous cycles, as the clock runs continuously.

Regarding claims 9 and 18, Matsuzaki teaches all subject matter claimed, as applied to claim 8. Matsuzaki further teaches the step of providing an offset (output of 15, d-l-clk, as the reference signal is adjusted by the variable delay) in the reference signal prior to the step of adjusting (13), which is to minimize the worst-case scew introduced between the reference clock signal and the generated clock signal, since the offset is adjusted to reduce the offset.

Regarding claim 17, Matsuzaki teaches all subject matter claimed, as applied to claim 8. Matsuzaki further teaches wherein the clock signal exhibits different frequencies during successive cycles, the energy of the clock signal being spread equally over the different frequencies. (note col.7, lines 52-59)

Regarding claim 19, Matsuzaki discloses a method for spreading the electromagnetic emissions of a generated clock signal that is created in response to a reference clock signal (see Fig.14), comprising the steps of providing a delay line (11) in the path of the reference clock signal, providing an adjustable delay trim units (570~579 in Fig.17) in the path of the reference clock signal, enabling a first, second, third set of delay trim units in the delay adjustable delay line during its respective clock period, thereby causing the generated clock signal to exhibit its respective clock period where the control signals (Q1~Q4) enables corresponding delay elements and determine the clock period. (note col.15, lines 16-34) Matsuzaki further discloses that the phase relations are predetermined with relation to the control signals shown in Fig.18. When the control signals are received by the controller (26 in Fig.14), a regular pattern (11111, 11110, 11101, 11100 ... and so on) with out any unknown patterns when received by the delay elements are sent to the delay elements for adjustment.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki (cited previously) in view of Hardin.

Regarding claim 21, Matsuzaki teaches all subject matter claimed, as applied to claim 20. Matsuzaki teaches the adjustable delay line providing a generated clock signal. However, Matsuzaki does not explicitly teach wherein the clock signal exhibits different frequencies during successive clock cycles where the energy of the generated clock signal being spread over the different frequencies. Hardin teaches, in the same field of endeavor, having reference frequency generator (15 in Fig.1) output to a spread spectrum clock generator (14). Hardin teaches the limitation of having different frequencies during successive clock cycles where the energy of the generated clock signal is spread over the different frequencies. (note col.4, lines 8-55) Therefore, it would have been obvious to one skilled in the art at the time of the invention to connect Matsuzaki's teaching to the spread spectrum clock generator of Hardin and generate a new clock signal for the purpose of suppressing EMI emissions. (note col.2, lines 33-63)

### ***Response to Arguments***

3. Applicant's arguments filed on 3/3/04 have been fully considered but they are not persuasive.

Regarding claim 8, applicants argue that the control signals Q0~Q4 are not predetermined patterns and can exhibit many different patterns during consecutive clock cycles. As explained above, Q0~Q4 are predetermined patterns, where Matsuzaki illustrates in Fig.18. The examiner agrees that the patterns are determined by the phase difference, however, each pattern (11111

or 11110 or 11101...and so on) are predetermined. (note col.1, lines 4-10 and col.15, lines 35-60) The digits of 11111 may be considered as one pattern where 11110 is another pattern. Depending on the count up and count down value, a predetermined pattern is implemented to adjust the delay elements.

And further, during the clock cycles where phase differences are detected by the phase detector (16), Q0~Q4 of predetermined patterns are generated for the term of the consecutive clock cycles.

***Allowable Subject Matter***

4. Claims 1-7 are allowed.
5. Claims 10-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is a statement of reasons for the indication of allowable subject matter:  
Applicants disclose a method for spreading the electromagnetic emissions of a generated clock comprising a spread generator generating a predetermined pattern. A clock generator, an adder and plurality of delay elements. The predetermined pattern and output of the clock generator are combined, which is used as an input to the delay elements. The output of the delay elements are used as a newly generated clock signal wherein the newly generated clock signal has different clock periods in its respective clock cycle in a repeating pattern. Closest prior art, Matsuzaki, teach all subject matter claimed. However, Matsuzaki does not teach

wherein the clock signal generated has different clock periods and different clock cycle in a repeating pattern. Matsuzaki teaches adjustment of phase error, but does not teach generating clock signals with different clock periods in a predetermined pattern.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Sam Ahn** whose telephone number is **(703) 305-0754**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

**Any response to this action should be mailed to:**



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Art Unit: 2634

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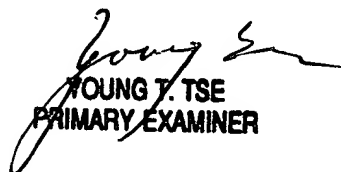
**or faxed to:**

**(703) 872-9306**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Sam K. Ahn  
5/26/04

  
YOUNG T. TSE  
PRIMARY EXAMINER